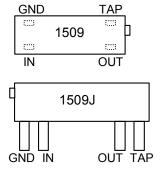
MECHANICALLY VARIABLE DELAY LINE (SERIES 1509 & 1509J)



FEATURES PACKAGES

- Ideal for "Set and Forget" applications
- Multi-turn adjustment screw (1509: 20 turns, 1509J: 60 turns)
- Stackable for PC board economy
- Fits standard 14-pin DIP socket (1509)
- 20mil x 10mil flat leads (1509)
- #20 gauge leads (1509J)
- Resolution: As low as 0.15ns
- Dielectric breakdown: 50 Vdc Temperature coefficient: 200 PPM/°C



1509-xxz 1509J-xxz

> $xx = Max Delay (T_D)$ z = Impedance Code

FUNCTIONAL DESCRIPTION

The 1509- and 1509J-series devices are mechanically variable, passive delay lines. The signal input (IN) is reproduced at the tap output (TAP), shifted by an amount which can be adjusted between 0 and T_D, where T_D is the device dash number. The fixed output (OUT) reproduces the input, delayed by T_D, and must be terminated to match the characteristic impedance of the line, which is

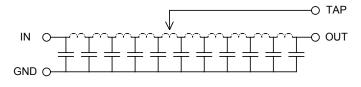
PIN DESCRIPTIONS

IN Signal Input **TAP** Variable Output OUT **Fixed Output GND** Ground

given by the letter code that follows the dash number (See Table). The tap output is unbuffered. The 3dB bandwidth of the line is given by 0.35 / T_R, where T_R is the rise time of the line (See Table).

300

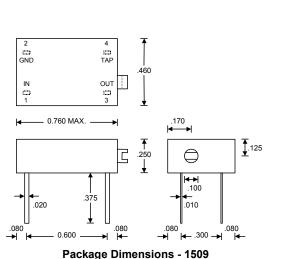
SERIES SPECIFICATIONS

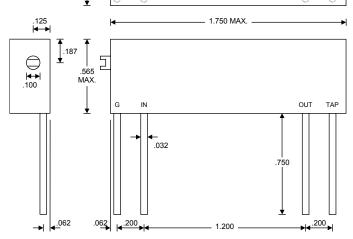


Functional Diagram

DASH NUMBER SPECIFICATIONS

Part Number	Max Dly (ns)	TR (ns)	Imped (Ω)	RDC (Ω)
1509-05B	5	3	100	0.4
1509-20C	20	8	200	1.0
1509-20D	20	8	250	1.0
1509J-10B	10	4	100	0.8
1503.I-40C	40	a	200	15





Package Dimensions - 1509J

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PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

INPUT: OUTPUT:

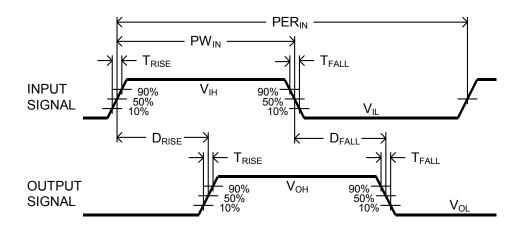
Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ R_{load} : $10\text{M}\Omega$ Input Pulse:High = 3.0V typical C_{load} :10pfLow = 0.0V typicalThreshold:50% (Rising & Falling)

Source Impedance: Low = 0.0V typical 50Ω Max.

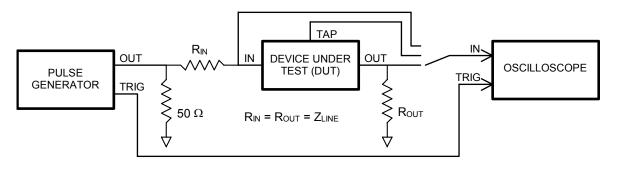
Rise/Fall Time: 3.0 ns Max. (measured

at 10% and 90% levels)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup